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60. [redacted]

61. [redacted]

62. [redacted]

63. [redacted] The data sheet for this part is publicly available and known in the industry.

**Exhibit D: NAND Customer Requirements Spreadsheet, and NAND Channel Assignments**

NAND Customer Requirements

64. Pochowski Declaration Exhibit D (repeated in Lai Exhibit A) contains [redacted]

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[redacted]

65. As a specific example I review the Hynix HY27UH08AG(5/D)M Series 16Gbit NAND Flash device. Attached as exhibit SS is a true and correct copy of the HY27UH08AG(5/D)M Series 16Gbit NAND Flash device upon which this analysis is based. ("the Datasheet").

a. [redacted]

NAND Channel Assignments

67. Pochowski Exhibit D (repeated in Lai Exhibits B, C, and D) [redacted]. Verigy claims trade secret status. The diagrams [redacted] These diagrams are so common that they are often included in Semiconductor test patents. (see previously discussed patents for examples). To create a channel assignment it's author need only have knowledge of the pins of the DUT, which are typically published by semiconductor manufacturers in their publicly available datasheets.

68 [redacted]

**Exhibit E: Mock Presentation to [redacted] Simulations**

[redacted]

[redacted] in the MS Power Point presentation (Exhibit E of the Pochowski Declaration) appear generated from industry standard parameters. For example:

a. The standard diameter of a probe card is 400mm. From this knowledge one can estimate that a typical trace length from any circuitry mounted on the probe (such as Flash Enahncer) to the wafer is approximately eight (8) inches.

b. The typical resistance and capacitance for a FET switch are 5 ohms and 1 Pico Farad, respectively.

c. DUT input capacitance is typically modeled as 5 pico Farads. This standard value can be confirmed from IBIS (Input/Output Buffer Information Specification) models commonly available in the industry. An article describing the IBIS models can be found is attached as Exhibit JJ, which was downloaded from the World Wide Web at http://www.eetasia.com/ARTICLES/2005JUN/A/2005JUN01_CTRLD_AN08.PDF?SOURCES=DOWNLOAD.

d. Many NAND flash testers today operate in the range of 50 - 100 Mega Hertz. This specification is known in the industry and is also available on many website. Such an assumption is also consistent with known Flash Memory chip speeds, which are readily available in datasheets from any Flash Memory manufacturer's website. See http://www.evaluationengineering.com/archive/articles/1000focus.htm for an example of the V4400 100MHz test speed. A copy of the article is attached as Exhibit RR.

[redacted]

[3] See http://en.wikipedia.org/wiki/Switch for a description of switches and how they work.
[4] Blanchard Declaration para A, exhibit E, F.(Honeywell and other semiconductor switch datasheets)
[5] Blanchard Declaration, para B, exhibits G, H (micron patents on probe card multiplexing)

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70. [redacted]

72. [redacted] For example, in simulating wafer testing:

a. [redacted]

73 [redacted]

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76. [redacted]

[redacted] (Exhibit to Leventhal Declaration)

78 [redacted]

80. This type of switch technology is well known in the industry. Data sheets from other companies that discuss similar switch technology are listed below.

a. Peregrine SP4T, SP7T (true and correct copy attached as Exhibit L)

b. Hetlite SP4T (true and correct copy attached as Exhibit M)

c. RFMD SP4T (true and correct copy attached as Exhibit N)

d. Skyworks SP4T (true and correct copy attached as Exhibit O)

e. Tyco SP4T (true and correct copy attached as Exhibit P)

81. Flash Enhancer is not derived from the Chameleon ASIC. A detailed discussion of this can be found in the section below.

[redacted]

82. The Disclosure describes desires for problems that an application specific integrated circuit ("ASIC") could solve for testing if mounted on a probe card. Here, I consider whether each assertion of the Disclosure is publicly available or well known in the industry, and whether each assertion is now present in Flash Enhancer. I consider each section of the Disclosure in turn.

Section B of the Disclosure

83. [redacted]

i. This is not an invention. Fan out of bi-directional I/O (data) lines is disclosed in the '112 Micron Patent, and the '225 FormFactor patent.

ii. Flash Enhancer includes this capability.

[redacted]

i. This is not an invention. The ability to disconnect a shorted/failed DUT is disclosed in the '112 Micron Patent, and the '225 FormFactor patent.

ii. Flash Enhancer includes this capability.

[redacted]

i. This is not an invention. Fan out of power supplies is commonly done in the ATE industry today through the use of mechanical relays, photoMOS relays, and FET switches placed on load boards and probe cards.

ii. [redacted]

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i. This is not an invention. Fan out of VCC sense lines is currently done in the industry by using the same FETs that are used for the signal lines. The standard off-the-shelf specs for the Honeywell HRF-1000 demonstrate that Honeywell's FETs can be used for this application.

ii. [redacted] capability.

e. [redacted]

i. [redacted] Therefore, this is not an invention.

ii. [redacted]

f. [redacted]

i. [redacted]

ii. [redacted]

g. [redacted]

i. As discussed previously, combining multiple switches into a single ASIC would be obvious to any engineer in the testing industry. This concept is well known in the industry. Therefore, this is not an invention.

ii. [redacted]

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[redacted]

Section C of the Disclosure

k. [redacted]

i. This is not an invention. The '112 Micron patent discloses exactly an invention that can double or quadruple the entire array of tester resources.

ii. The '112 Micron patent discloses one embodiment that uses 100% solid state technology.

iii. [redacted]

Section D of the Disclosure

l. Concepts: [redacted]

i [redacted] an invention. [redacted]

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[redacted]

84. I conclude that all of the concepts asserted in the Disclosure are either publicly available or known in the industry. [redacted]

[redacted] in

Section B of the Filed Disclosure

86. Section B is essentially identical to the prior disclose for the first ten (10) conceptual assertions. I assess the additional concepts asserted here:

a. Concept 11. [redacted]

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ii. [redacted]